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EXAMINER	
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ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,074	MANTL, SIEGFRIED	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,10-39,42-45,48,50-79 and 90-98* is/are pending in the application.

4a) Of the above claim(s) *90-96* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-21,24,26,27,42-43,45,48,50,51,54,56-65,67,74,75,79 and 97-98* is/are rejected.

7)☒ Claim(s) *22,25,28,32,35-37,39,52,53,55,66,68-73 and 76-78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3 and 58 are objected to because of the following informalities: :

Regarding claim 3, "the layer structure" lacks of antecedent basis.

Regarding claim 58, in the claimed feature "a thickness d4 close to a critical layer thickness" is unclear as to "close to" meaning not clear.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 54 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 54, claimed feature "noticeable relaxation" is unclear. It's not clear the "relaxation" is not "noticeable" to whom--to a computer test, a person looking with a magnifier, or a person looking with bare eyes.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-5,10-14,18-21,45,48,50,54,56-65,74, 75,79, and 97-98 are rejected under 35 U.S.C. 102(e) as being anticipated by Shih et al (PG Pub 2003/0077882 A1).

5. Regarding claim 1, Shih teaches a method of converting a silicon on insulator (SOI) substrate into a strained SOI layer on substrate, the method comprising the steps of: providing an SOI substrate having a thin silicon layer (layer 14' in fig. 3) and an insulator (layer 12); providing at least one first epitaxial relaxing layer (layer 20) on the SOI-substrate, producing a defect region in a layer (layer 16) above the silicon layer of the SOI-substrate, and relaxing the layer above the silicon layer by a thermal treatment to simultaneously strain the silicon layer of the SOI-substrate via dislocation mediated strain transfer and to produce the strained silicon layer directly on the insulator (see paragraph [0023]). Note that the device in current application and Shih's device have the same structure—a silicon germanium layer formed on an SOI, the silicon germanium layers having the same concentration (see page 36 of the current application and paragraph [0019] of Shih), the silicon germanium layers having the same thickness (see layer 4 of current application or paragraphs [0066], [0069] and [0111] of PG Pub of current application and paragraph [0019] of Shih). Both devices are also annealed at the same temperature (page 18 of current application and paragraph [0021] of Shih). Thus, Si 14' in Shih is also a strained layer as claimed.

6. Regarding claim 2, Shih teaches the method according to claim 1, further comprising the step of forming defects (layer 16 in fig. 4, paragraph [0021]) that give rise to relaxation of at least one neighboring layer of the layer which is to be strained.

7. Regarding claim 3, Shih teaches the method according to claim 1, further comprising the step of subjecting the layer (layer 16 in fig. 4) for relaxation to a thermal treatment (paragraph [0021]).

8. Regarding claim 4, Shih teaches the method according to claim 1, further comprising the step of depositing the first layer (layer 16 in fig. 4) upon the silicon layer to be strained.

9. Regarding claim 5, Shih teaches the method according to claim 4 wherein the first layer has a different degree of stress than the silicon layer to be strained. Note that layers 14' and 16 have different lattice constants thus they undergo different degrees of stress from each other.

10. Regarding claim 10, Shih teaches the method according to claim 1 wherein two neighboring layers (layers 16 and 20 in fig. 5) of the layer to be strained have other degrees of stress than the layer to be strained. Note that layers 14', 16, and 20 have different lattice constants thus they undergo different degrees of stress from one another.

11. Regarding claim 11, Shih teaches the method according to claim 1 wherein a plurality of layers (layers 16' and 20 in fig. 5, see paragraph [0025]) are relaxed.

12. Regarding claim 12, Shih teaches the method according to claim 1 wherein a plurality of layers (layers 14' and 22 in fig. 6, see paragraphs [0020] and [0026]) to be strained have strain transferred to them.

13. Regarding claim 13, Shih teaches the method according to claim 1, further comprising the step of depositing on the first layer (layer 16 in fig. 6) epitaxially at least one second layer (layer 22) with a different lattice structure.

14. Regarding claim 14, Shih teaches the method according to claim 13 wherein the defect region (strain in layer 22, see paragraph [0026]) is produced in the second layer.

15. Regarding claim 18, Shih teaches the method according to claim 1, further comprising the step of depositing an epitaxial layer structure comprising a plurality of layers (layers 16 and 20 in fig. 5) on the substrate.

16. Regarding claim 19, Shih teaches the method according to claim 1, further comprising the step of relaxing the first layer (layer 16 in fig. 5, see paragraph [0021]) by a thermal treatment.

17. Regarding claim 20, Shih teaches the method according to claim 19 wherein the thermal treatment is done at a temperature between 550 degrees and 1200 degrees C (see paragraph [0021]).

18. Regarding claim 21, Shih teaches the method according to claim 19 wherein the thermal treatment is done at a temperature between 700 degrees and 980 degrees C (see paragraph [0021]).

19. Regarding claim 45, Shih teaches the method according to claim 1 wherein the layer neighboring the silicon layer becomes viscous at a temperature required for the

relaxation. Note that Shih device is anneal at the temperature disclosed in current application. Thus, the silicon layer in Shih's device is also viscous at the anneal temperature.

20. Regarding claim 48, Shih teaches the method according to claim 1 Si-Ge (layer 16 in fig. 5) as the material for the first layer which is deposited on the layer to be strained.

21. Regarding claim 50, Shih teaches the method according to claim 13 wherein silicon (layer 22 in fig. 6) as the material for the second layer which is deposited upon the first layer.

22. Regarding claim 54, Shih teaches the method according to claim 1 wherein the total layer thickness of the layer structure is so selected that during growth of the applied epitaxial layer s these it does not produce any noticeable relaxation. Since the device is nanoscale in size, no one can notice with bare eyes.

23. Regarding claim 56, Shih teaches the method according to claim 1 wherein a layer (layer 14' in fig. 5) to be strained has a thickness d3 in the range of 1 to 50 nanometers (see paragraph [0016]).

24. Regarding claim 57, Shih teaches the method according to claim 1 wherein the silicon layer (layer 14' in fig. 5) to be strained has a thickness d3 in the range of 5 to 30 nanometers (paragraph [0016]).

25. Regarding claim 58, Shih teaches the method according to claim 57 wherein the first layer (layer 16, see paragraph [0023]) has a thickness d4 close to a critical layer thickness for pseudomorphic growth.

26. Regarding claim 59, Shih teaches the method according to claim 58 wherein a layer thickness ratio d4/d3 is greater than about 10. See paragraphs [0019] and [0016] for layer 16 with thickness of 100nm and layer 14' with thickness of 10nm.

27. Regarding claim 60, Shih teaches the method according to claim 13 wherein the second layer (layer 20 in fig. 5, see paragraph [0024]) has a thickness ds = 50 nanometer to 1000 nanometer.

28. Regarding claim 61, Shih teaches the method according to claim 13 wherein the second layer (layer 20 in fig. 5, see paragraph [0024]) has a thickness ds = 300 nanometer to 500 nanometer.

29. Regarding claim 62, Shih teaches the method according to claim 1 wherein the layer to be strained is locally strained (strained within layer 16).

30. Regarding claim 63, Shih teaches the method according to claim 62 wherein the layer to be strained (in layer 14' in fig. 5) is locally strained in regions which are vertical in a plane with the defect region (in layer 16).

31. Regarding claim 64, Shih teaches the method according to claim 13 wherein the defect region (in layer 16 in fig. 5) is produced at a spacing (thickness of layer 20, which is in the range of 100nm to 400nm, see paragraph [0024]) of 50 nanometers to 500 nanometers from the layer to be relaxed.

32. Regarding claim 65, Shih teaches the method according to claim 1 wherein the defect region (in layer 20 in fig. 5) is at a spacing (thickness of layer 16', also see paragraph [0019]) of 50 nanometers to 100 nanometers above the first layer (layer 16) on the layer to be strained.

33. Regarding claim 74, Shih teaches the method according to claim 1, further comprising the step of producing on a strained region of the layer an n- and/or p-MOSFET (see source and drain region in paragraph [0028]).

34. Regarding claim 75, Shih teaches the method according to claim 1, further comprising the step of depositing a further epitaxial layer comprising silicon (layer 22 in fig. 6) layer.

35. Regarding claim 79, Shih teaches the method according to claim 1, wherein the steps of claim 1 are carried out a plurality of times (when more than one device is produced).

36. Regarding claim 97, Shih teaches a method of converting a silicon on insulator (SOI) substrate into a strained SOI substrate, the method comprising the steps of: providing an SOI substrate with a thin silicon layer (layer 14' in fig. 5) and an insulator (layer 12); providing only one first relaxing layer (layer 16) on the SOI-substrate; producing a defect region (see paragraphs [0020] and [0021]) in the first layer above the silicon layer; and relaxing the first layer above the silicon layer to simultaneously strain the thin silicon layer of the SOI-substrate via dislocation mediated strain transfer to produce the strained silicon layer directly on the insulator. Note that the device in current application and Shih's device have the same structure—a silicon germanium layer formed on an SOI, the silicon germanium layers having the same concentration (see page 36 of the current application and paragraph [0019] of Shih), the silicon germanium layers having the same thickness (see layer 4 of current application or paragraphs [0066], [0069] and [0111] of PG Pub of current application and paragraph

[0019] of Shih). Both devices are also annealed at the same temperature (page 18 of current application and paragraph [0021] of Shih). Thus, Si 14' in Shih is also a strained layer as claimed.

37. Regarding claim 98, Shih teaches a method of converting a silicon on insulator (SOI) substrate into a strained SOI substrate, the method comprising the steps of: providing an SOI substrate having a silicon layer (layer 14') and an insulator (layer 12); providing a first relaxing layer (layer 16) on the SOI substrate; epitaxially forming a second layer (layer 20) with a different structure (layer 20 has a different structure than that of layer 14') on the first layer; producing a defect region (in layer 20 due to different lattice constants between layers 20 and 22, see paragraph [0026]) in the second layer; and relaxing the first layer to simultaneously strain the silicon layer of the SOI substrate via dislocation mediated strain transfer and to produce the strained silicon layer directl7 on the insulator. Note that the device in current application and Shih's device have the same structure—a silicon germanium layer formed on an SOI, the silicon germanium layers having the same concentration (see page 36 of the current application and paragraph [0019] of Shih), the silicon germanium layers having the same thickness (see layer 4 of current application or paragraphs [0066], [0069] and [0111] of PG Pub of current application and paragraph [0019] of Shih). Both devices are also annealed at the same temperature (page 18 of current application and paragraph [0021] of Shih). Thus, Si 14' in Shih is also a strained layer as claimed.

38. Claims 1-5,15-17,19-20,24,26-27,42-43,45,48,51,54,56-57,62-63,67,74,79,97 are rejected under 35 U.S.C. 102(e) as being anticipated by Cohen et al (PG Pub 2004/0142541 A1).

39. Regarding claim 1, Cohen teaches a method of converting a silicon on insulator (SOI) substrate into a strained SOI layer on substrate, the method comprising the steps of: providing an SOI substrate having a thin silicon layer (layer 100 in fig. 2) and an insulator (layer 150); providing at least one first epitaxial relaxing layer (layer 110) on the SOI-substrate, producing a defect region in a layer (defects in layer 110 produced by He implants, see paragraph [0026]) above the silicon layer of the SOI-substrate, and relaxing the layer above the silicon layer by a thermal treatment to simultaneously strain (see figs. 4-7, see paragraphs [0027] to [0032]) the silicon layer of the SOI-substrate via dislocation mediated strain transfer and to produce the strained silicon layer directly on the insulator. Note that although the final SiGe layer 520 is referred by as "strained" by Cohen (see paragraph [0030]), this "strained" layer should have the same structure as the claimed layer—"the layer above the silicon layer" by relaxing "the layer" since the claimed device and that disclosed by Cohen are formed by the same process--Si implantation in a SiGe layer formed on a Si layer of a SOI substrate and thermal treatment (see the third embodiment on page 37 and 38 of current application, and paragraphs [0028] and [0030] of Cohen). In fact, the SiGe layer of the current application and that of Cohen's may be view as both strained and relaxed because SiGe and pure Si have different lattice constants. At the Si/SiGe interface, the Si layer

and the SiGe layer are strained. Away from the Si/SiGe interface, the SiGe layer relax to its natural state.

40. Regarding claim 2, Cohen teaches the method according to claim 1, further comprising the step of forming defects (the SiGe layer 110 in fig. 2) that give rise to relaxation of at least one neighboring layer of the layer which is to be strained.

41. Regarding claim 3, Cohen teaches the method according to claim 1, further comprising the step of subjecting the layer for relaxation to a thermal treatment (annealing, see paragraph [0030]).

42. Regarding claim 4, Cohen teaches the method according to claim 1, further comprising the step of depositing the first layer (layer 110 in fig. 2) upon the silicon layer (layer 100) to be strained.

43. Regarding claim 5, Cohen teaches the method according to claim 4 wherein the first layer has a different degree of stress than the silicon layer to be strained. Note that SiGe is compressed since it has larger lattice constant than that of Si. Si layer experiences tensile strain.

44. Regarding claim 15, Cohen teaches the method according to claim 1 wherein on the layer to which strain is to be transferred at least one graded layer (SiGe layer 110 in fig. 2, see paragraph [0026]) is deposited as the first layer.

45. Regarding claim 16, Cohen teaches the method according to claim 15 wherein at the region of the layer to be strained, the graded layer has a degree of strain that is different from that of the layer to be strained. Note that SiGe is compressed since it has larger lattice constant than that of Si. Si layer experiences tensile strain.

46. Regarding claim 17, Cohen teaches the method according to claim 15, further comprising the step of producing a defect region in the graded layer (SiGe layer 110 in fig. 2, see paragraph [0026]).

47. Regarding claim 19, Cohen teaches the method according to claim 1, further comprising the step of relaxing the first layer by a thermal treatment (see paragraph [0030]).

48. Regarding claim 20, Cohen teaches the method according to claim 19 wherein the thermal treatment is done at a temperature between 550 degrees and 1200 degrees C (see paragraph [0008]).

49. Regarding claim 24, Cohen teaches the method according to claim 1 wherein the relaxation is carried out over a limited region of a layer (top region of SiGe in fig. 2, see rejection in claim 1).

50. Regarding claim 26, Cohen teaches the method according to claim 1 wherein the defect region is produced by ion implantation (see paragraph [0026]).

51. Regarding claim 27, Cohen teaches the method according to claim 26 wherein for the implantation, hydrogen ions or helium ions are used (see paragraph [0026]).

52. Regarding claim 42, Cohen teaches the method according to claim 1 wherein a silicon surface layer of the SOI substrate is the layer to be strained and the SiO_2 (insulator 150 in fig. 2) of the SOI substrate forms the insulator of the substrate.

53. Regarding claim 43, Cohen teaches the method according to claim 1 wherein an SIMOX (see paragraph [0025]) or BESOI substrate is selected as a base structure for the substrate.

54. Regarding claim 45, Cohen teaches the method according to claim 1 wherein the layer neighboring the silicon layer becomes viscous (SiGe layer becomes amorphous, see paragraphs [0029] to [0030]) at a temperature required for the relaxation.

55. Regarding claim 48, Cohen teaches the method according to claim 1 Si-Ge (layer 110 in fig. 2) or Si-Ge-C or Si-C as the material for the first layer which is deposited on the layer to be strained.

56. Regarding claim 51, Cohen teaches the method according to claim 15, further comprising the step of selecting Si-Ge (layer 110 in fig. 2, see paragraph [0026]) as the material for a graded layer.

57. Regarding claim 54, Cohen teaches the method according to claim 1 wherein the total layer thickness of the layer structure is so selected that during growth of the applied epitaxial layer s these it does not produce any noticeable relaxation. Since the device is nanoscale in size, no one can notice with bare eyes.

58. Regarding claim 56, Cohen teaches the method according to claim 1 wherein a layer (layer 100 in fig. 2, paragraph [0025]) to be strained has a thickness d3 in the range of 1 to 50 nanometers.

59. Regarding claim 57, Cohen teaches the method according to claim 1 wherein the silicon layer (layer 100 in fig. 2, paragraph [0025]) to be strained has a thickness d3 in the range of 5 to 30 nanometers.

60. Regarding claim 62, Cohen teaches the method according to claim 1 wherein the layer to be strained is locally strained (strained within layer 100).

61. Regarding claim 63, Cohen teaches the method according to claim 62 wherein the layer to be strained is locally strained in regions which are vertical in a plane (the plane in Si layer 100 see fig. 2) with the defect region (in layer 110).

62. Regarding claim 67, Cohen teaches the method according to claim 1 wherein wet chemical material-selective etching is used (paragraph [0031]).

63. Regarding claim 74, Cohen teaches the method according to claim 1, further comprising the step of producing on a strained region of the layer an n- and/or p-MOSFET (see paragraph [0007]).

64. Regarding claim 79, Cohen teaches the method according to claim 1, wherein the steps of claim 1 are carried out a plurality of times (to make more than one strained SOI substrate).

65. Regarding claim 97, Cohen teaches a method of converting a silicon on insulator (SOI) substrate into a strained SOI substrate, the method comprising the steps of: providing an SOI substrate with a thin silicon layer (layer 100 in fig. 2) and an insulator (layer 150); providing only one first relaxing layer (layer 110) on the SOI-substrate; producing a defect region (defects in layer 110) in the first layer above the silicon layer; and relaxing the first layer above the silicon layer to simultaneously strain the thin silicon layer of the SOI-substrate via dislocation mediated strain transfer to produce the strained silicon layer directly on the insulator. Note that although the final SiGe layer 520 is referred by as "strained" by Cohen (see paragraph [0030]), this "strained" layer should have the same structure as the claimed layer—"the layer above the silicon layer" by relaxing "the layer" since the claimed device and that disclosed by Cohen are formed

by the same process--Si implantation in a SiGe layer formed on a Si layer of a SOI substrate and thermal treatment (see the third embodiment on page 37 and 38 of current application, and paragraphs [0028] and [0030] of Cohen). In fact, the SiGe layer of the current application and that of Cohen's may be view as both strained and relaxed because SiGe and pure Si have different lattice constants. At the Si/SiGe interface, the Si layer and the SiGe layer are strained. Away from the Si/SiGe interface, the SiGe layer relax to its natural state.

Response to Arguments

66. Applicant's arguments with respect to claims 1-98 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

67. Claims 22,25,28,32,35-37,39,52-53,55,66,68-73,76-78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

68. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Feifei Yeung-Lopez/
Examiner, Art Unit 2826

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